In the Claims:

Please amend claim 1. Please add new claims 29 and 30. The claims are as follows:

1. (Currently Amended) A method of forming a semiconductor interconnect comprising, in the order recited:

(a) providing a semiconductor wafer;

(b) forming bonding pads in a terminal wiring level on the frontside of said wafer;

(c) reducing the thickness of said wafer prior to any dicing operationon said semiconductor wafer;

(d) forming solder bumps on said bonding pads; and

(e) dicing said wafer into individual bumped semiconductor chips.

2. (Original) The method of claim 1, wherein said solder bumps are formed by evaporation through a mask.

3. (Original) The method of claim 2, wherein said solder bumps includes material selected from the group consisting of 95% lead and 5% tin, 97% lead and 3% tin, 100% lead, lead alloys, 100% tin and tin alloys.

4. (Original) The method of claim 2, wherein said mask comprises molybdenum.

5. (Original) The method of claim 1, further including, between steps (c) and (d), forming a pad limiting metallurgy layer on said bonding pads.

6. (Original) The method of claim 5, wherein said pad limiting metallurgy layer is formed by evaporation through a mask.

7. (Original) The method of claim 5, wherein said pad limiting metallurgy includes materials selected from the group consisting of titanium nitride, copper, gold, titanium-tungsten, chrome, chrome-copper or combinations thereof.

8. (Original) The method of claim 6, wherein said mask comprises molybdenum.

9. (Original) The method of claim 5, wherein said pad limiting metallurgy is formed by evaporation through a mask and said solder bumps are formed by evaporation through said mask after said evaporation of said pad limiting metallurgy.

10. (Original) The method of claim 1, wherein step (c) is performed by a process selected from the group consisting of grinding a backside of said wafer with a rotating diamond grindstone, etching said backside surface of said wafer with a mixture of hydrofluoric and nitric acids while rotating said wafer, lapping the backside of said wafer by introducing a slurry containing abrasive particles between the backside of said wafer and a rotating wheel and, chemical-mechanical-polishing.

11. (Original) The method of claim 1, further including between steps (d) and (e) annealing said wafer in order to reflow said solder bumps into semi-spherical shapes.

12. (Original) A method of forming a semiconductor interconnect comprising, in the order recited:

(a) providing a semiconductor wafer;

(b) forming bonding pads in a terminal wiring level on the frontside of said wafer;

(c) reducing the thickness of said wafer to produce a reduced thickness wafer;

(d) providing an evaporation fixture comprising a bottom ring, a shim, an evaporation mask and a top ring;

(e) placing said shim into said bottom ring;

(f) placing said reduced thickness wafer on said shim;

(g) placing on and aligning said mask to said reduced thickness wafer;

(h) placing said top ring over said mask and temporarily fastening said top ring to said bottom ring;

(i) evaporating solder bumps on said bonding pads through said mask;

(j) removing said reduced thickness wafer from said fixture; and

(k) dicing said reduced thickness wafer into bumped semiconductor chips.

13. (Original) The method of claim 12, wherein said solder bumps includes material selected from the group consisting of 95% lead and 5% tin, 97% lead and 3% tin, 100% lead, lead alloys, 100& tin and tin alloys.

14. (Original) The method of claim 12, wherein said mask comprises molybdenum.

15. (Original) The method of claim 12, further including, between steps (h) and (i), forming a pad limiting metallurgy layer on said bonding pads.

16. (Original) The method of claim 15, wherein said pad limiting metallurgy includes materials selected from the group consisting of titanium nitride, copper, gold, titanium-tungsten, chrome, chrome-copper or combinations thereof.

17. (Original) The method of claim 12, wherein step (c) is performed by a process selected from the group consisting of grinding a backside of said wafer with a rotating diamond grindstone, etching said backside surface of said wafer with a mixture of hydrofluoric and nitric acids while rotating the wafer, lapping said backside of said wafer by introducing a slurry containing abrasive particles between said backside of said wafer and a rotating wheel and, chemical-mechanical-polishing.

18. (Original) The method of claim 12, further including between steps (j) and (k), annealing said reduced thickness wafer in order to reflow said solder bumps into semi-spherical shapes.

19. (Original) The method of claim 12, wherein the combined thickness of said shim and said reduced thickness wafer after step (c) is substantially equal to the thickness of said wafer before performing step (c).

20. (Original) The method of claim 12, wherein step (e) includes:

determining a first thickness of said reduced thickness wafer; and

selecting a shim having a second thickness wherein the first thickness plus the second thickness is substantially equal to a thickness of a standard wafer said fixture is designed to hold without said shim being present, said standard wafer having a thickness greater than a thickness of said reduced thickness wafer.

21. (Original) The method of claim 12, wherein step (h) includes pressing peripheries of said mask, said reduced thickness wafer and an outer periphery of said shim a predetermined distance toward a surface of said bottom ring while an inner periphery of said shim is pressed against and interior portions of said reduced thickness wafer and said mask are pressed toward an interiorly located raised annular ring portion of said bottom ring, said annular ring portion extending from said surface of said bottom ring, in order to bow a central part of said reduced thickness wafer and mask away from said bottom ring and bow peripheral portions of said reduced thickness wafer and mask toward said bottom ring.

22. (Original) The method of claim 21, wherein step (h) includes selecting a shim of having a thickness such that said reduced thickness wafer is bowed the same amount as said wafer before performing step (c) would have been bowed without said shim being present.

23. (Original) The method of claim 21, wherein step (h) includes selecting a shim of having a thickness such that said reduced thickness wafer is bowed the same amount as a standard wafer said fixture is designed to hold without said shim being present would have been bowed without said shim being present, said standard wafer having a thickness greater than a thickness of said reduced thickness wafer.

24. (Original) The method of claim 12, wherein said fixture imparts a bow to said reduced thickness wafer and to said mask, a central part of said reduced thickness wafer and a central part of said mask bowed away from said bottom ring and peripheral portions of said reduced thickness wafer and said mask bowed toward said bottom ring.

25. (Withdrawn) A fixture for holding wafer and an evaporative mask comprising:

a bottom ring having a inner periphery and an outer periphery, said bottom ring having a raised inner lip formed along said inner periphery and a raised outer lip formed along said outer periphery, the height of said inner lip above a surface of said bottom ring being greater than a height of said outer lip above said surface of said bottom ring;

a shim having a inner and an outer periphery, the outer periphery of said shim fitting inside and in proximity to said outer lip of said bottom ring, a bottom surface of said shim proximate to said inner periphery of said shim contacting an upper surface of said inner lip of said bottom ring;

a top ring having an inner periphery and an outer periphery, said top ring having a lower raised lip formed along said inner periphery of said bottom ring and extending below a bottom surface of said top ring; and

said bottom ring and said top ring adapted to press a bottom surface of said wafer against an upper surface of said shim and to press a top surface of said wafer against a bottom surface of said mask and to press a top surface of said mask proximate to said periphery of said mask against a lower surface of said lower raised lip of said top ring.

26. (Withdrawn) The fixture of claim 25, wherein said shim, said top ring and said bottom ring are adapted to impart a bow to said wafer and said mask, a central part of said wafer and a central part of said mask bowed away from said bottom ring and peripheral portions of said wafer and said mask bowed toward said bottom ring.

27. (Withdrawn) The fixture of claim 25, wherein the combined thicknesses of said wafer and said shim are substantially equal to a thickness of a standard wafer said fixture is designed to hold without said shim being present, said standard wafer having a thickness greater than a thickness of said wafer.

28. (Withdrawn) The fixture of claim 25, wherein said shim has thickness such that said wafer is bowed the same amount as a standard thickness wafer would be bowed without said shim being present, said standard wafer having a thickness greater than a thickness of said wafer.

29. (New) The method of claim 1, wherein after step (c) semiconductor material is exposed on sidewalls and a bottom surface of each individual bumped semiconductor chip.

30. (New) The method of claim 1, further including, between steps (b) and (c):

forming one or more dielectric layers on said semiconductor substrate, said one or more dielectric layers covering said bonding pads; and

for each bonding pad, forming a via through said one or more dielectric layers to expose a top surface of each bonding pad, said one or more dielectric layers overlapping edges of each bonding pads.